CLAIMS

1. A device for reading a cell (4) of a memory, including a differential sense amplifier (18) having a first input terminal (16) connected to a cell column (10) and a circuit (34) intended to provide to a second input terminal (20) of the amplifier (18) a reference voltage (Vref), wherein said circuit (34) includes a means (38) for storing the voltage of said column and a means (38, 40, 42) for applying as a reference voltage (Vref) the stored voltage modified by a predetermined amount.

2. The device of claim 1, wherein the presence of a cell translates as a reduction in the voltage of a column and characterized in that the reference voltage is reduced by a predetermined amount with respect to the stored voltage.

3. The device of claim 1, wherein said circuit (34) includes a first capacitive element (38) intended to store the precharge voltage (Vpch) and a second capacitive element (40) connectable in parallel on the first one to set the value of the reference voltage (Vref).

4. The device of claim 3, wherein the capacitive elements are formed of the gate-source, gate-substrate, and gate-drain capacitances of MOS transistors.

5. The device of claim 1, wherein each column is associated with a precharge transistor (12) and in that the precharge transistors are addressable independently.

6. A method for reading a cell (4) of a memory, including the steps of:

- storing the voltage of a column just before reading; and

- modifying the stored voltage by a predetermined amount and using the modified voltage as a reference voltage.

7. The read method of claim 6, further consisting of comparing the reference voltage with a column voltage.

8. The reading method of claim 6, including the steps of:

- applying the precharge voltage (Vpch) on a first capacitor (38);

- disconnecting the first capacitor from the precharge voltage; and

- connecting in parallel on the first capacitor a second capacitor (40).